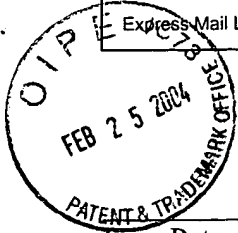


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Docket No.: 20046/0200815-USO
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Franz Hofmann et al.

Application No.: 10/768,971

Confirmation No.:

Filed: January 30, 2004

Art Unit: N/A

For: A FIN FIELD-EFFECT TRANSISTOR AND
METHOD FOR PRODUCING A FIN FIELD-
EFFECT TRANSISTOR

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed within three months of the U.S. filing date (37 CFR 1.97(b)(1)).

A copy of each document on the PTO/SB/08 is attached. Pursuant to the Notice issued by the United States Patent and Trademark Office dated July 11, 2003 waiving the requirements of 37 C.F.R. 1.98(a)(2)(i), copies of the United States Patents on PTO/SB/08a are not submitted.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is “prior art” for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed documents.

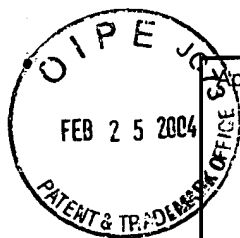
The Commissioner is authorized to charge any deficiency of up to \$300.00 or credit any excess in this fee to Deposit Account No. 04-0100.

Dated: February 25, 2004

Respectfully submitted,

By *[Signature]* ^{FLYNN BARRESON}
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Application No. (if known): 10/768,971

Attorney Docket No.: 20046/0200815-USO

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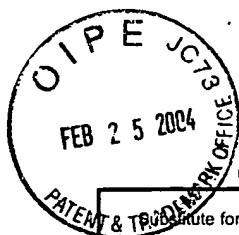
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/768,971
				Filing Date	January 30, 2004
				First Named Inventor	Franz Hofmann
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	20046/0200815-USO

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA	US-4,996,574-B1	02-26-1991	Shirasaki	
	AB	US-5,300,455-B1	04-05-1994	Vuillermoz et al.	
	AC	US-5,623,155-B1	04-22-1997	Kerber et al.	
	AD	US-5,915,183-B1	06-22-1999	Gambino et al.	
	AE	US-6,091,076-B1	07-18-2000	Deleonibus	
	AF	US-6,207,511-B1	03-27-2001	Chapman et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	CA	Fujiwara, A. et al: "Suppression of Unintentional Formation of Parasitic SI Islands on ASI Single-Electron Transistor by the Use of Sin Masked Oxidation"; Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Japan Society of Applied Physics. Tokyo, Japan, 1 September 1997, pages 482-483.		
	CB	Ishii, T. et al: "Characterization of One-Dimensional Conduction in an Ultra-Thin Poly-Si Wire"; Extended Abstracts of the International Conference on Solid State Devices and Materials", Japan Society of Applied Physics. Tokyo, Japan, 21 August 1995, pages 201-203.		
	CC	Hisamoto, Digh et al: "A Fully Depleted Lean-Channel Transistor (DELTA) - A Novel Vertical Ultrathin SOI MOSFET"; IEEE Electron Device Letters, Vol. 11, No. 1, January 1990, pages 36-38.		
	CD	Hisamoto, Digh et al: "A Folded-Channel MOSFET for Deep-sub-tenth Micron Era"; IEDM 98, pages 1032-1034, 1998.		
	CE	Kedzierski, Jakub et al: "Complementary silicide source/drain thin-body MOSFETS for the 20nm gate length regime"; IEDM 2000, pages 57-60.		

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